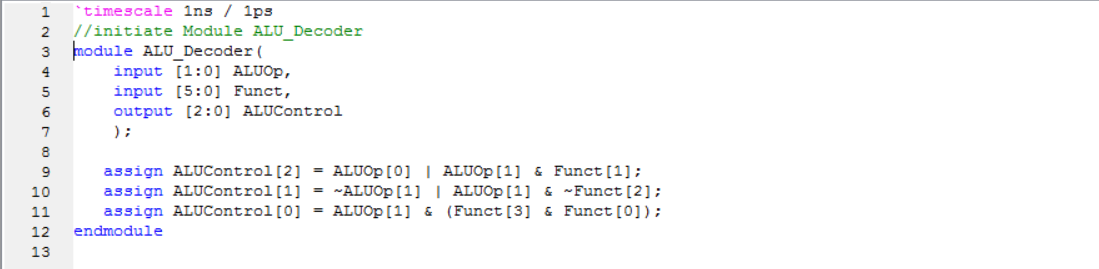
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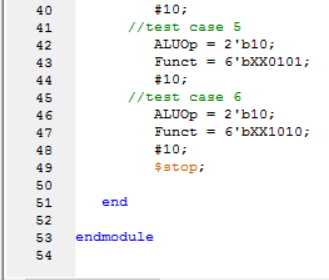
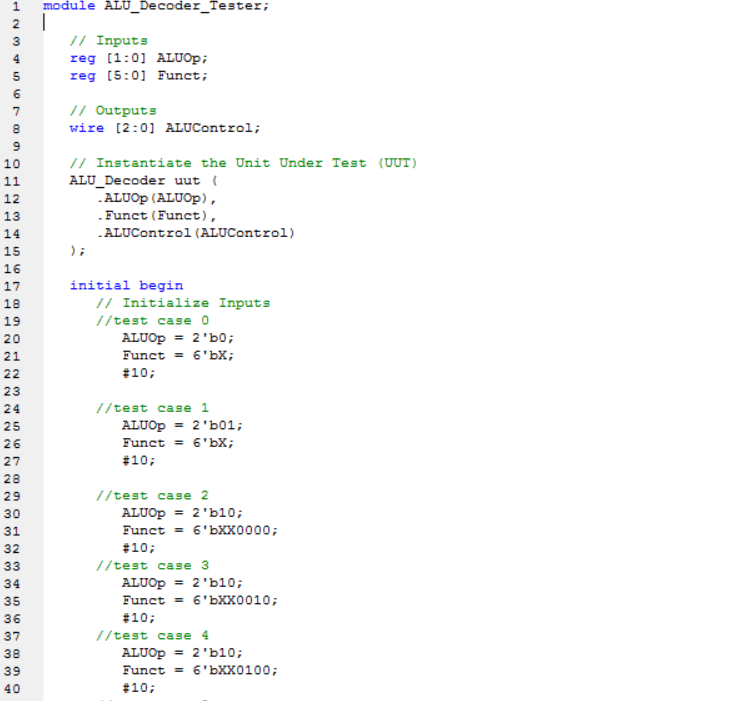
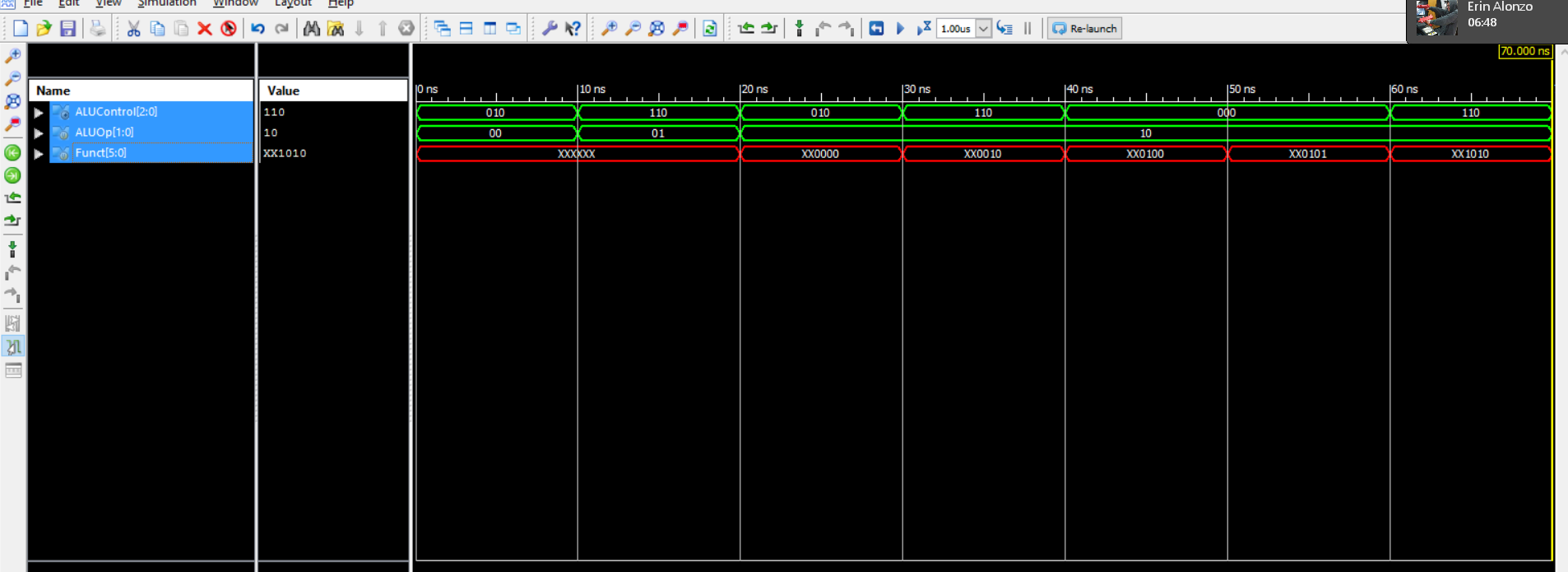
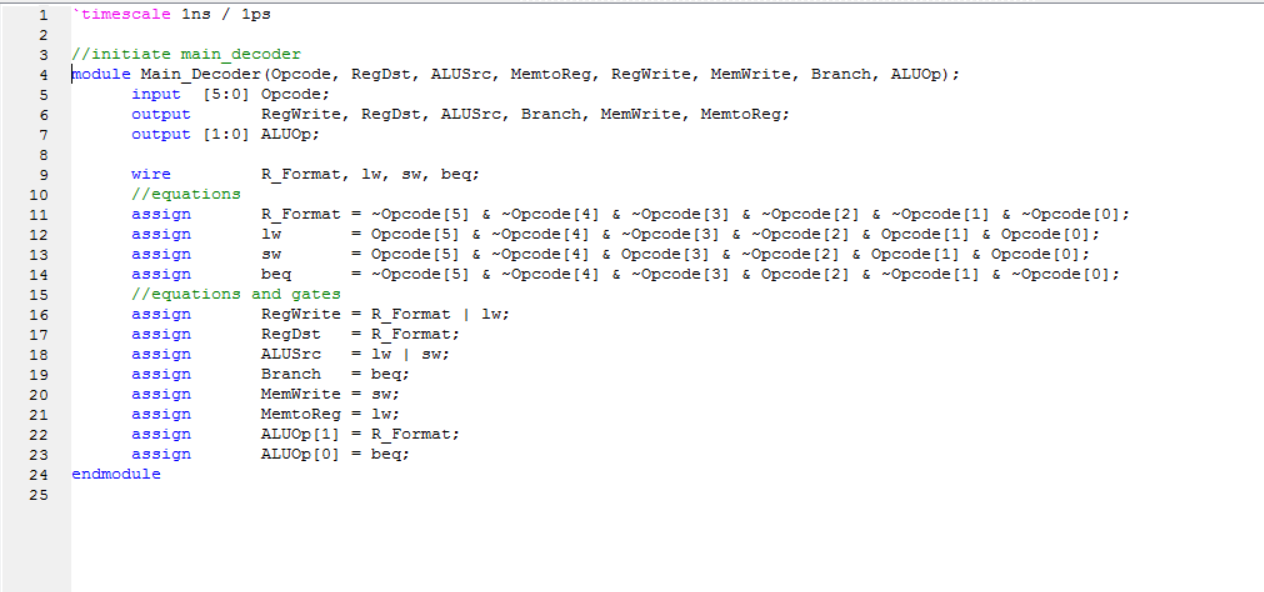
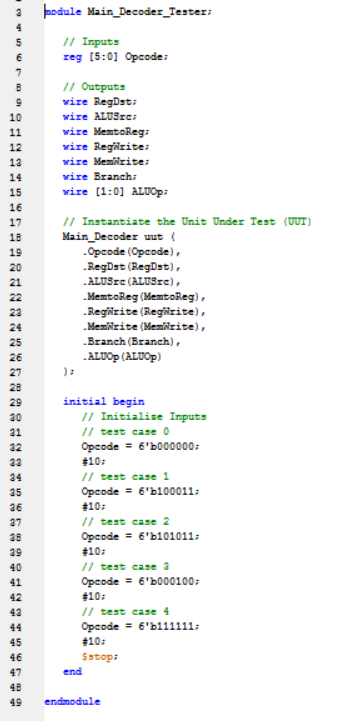
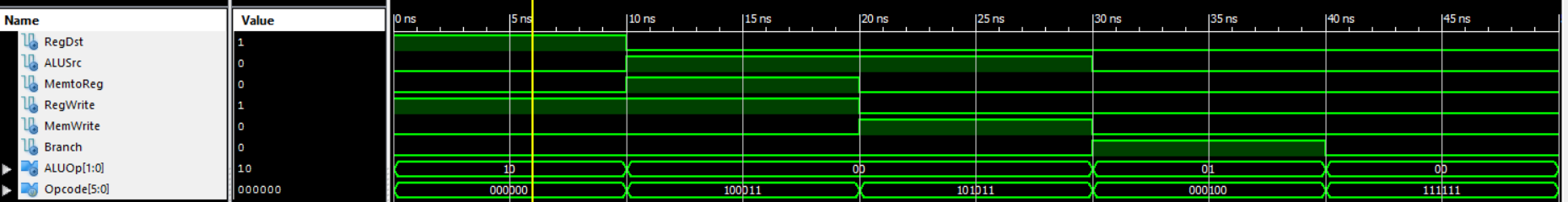
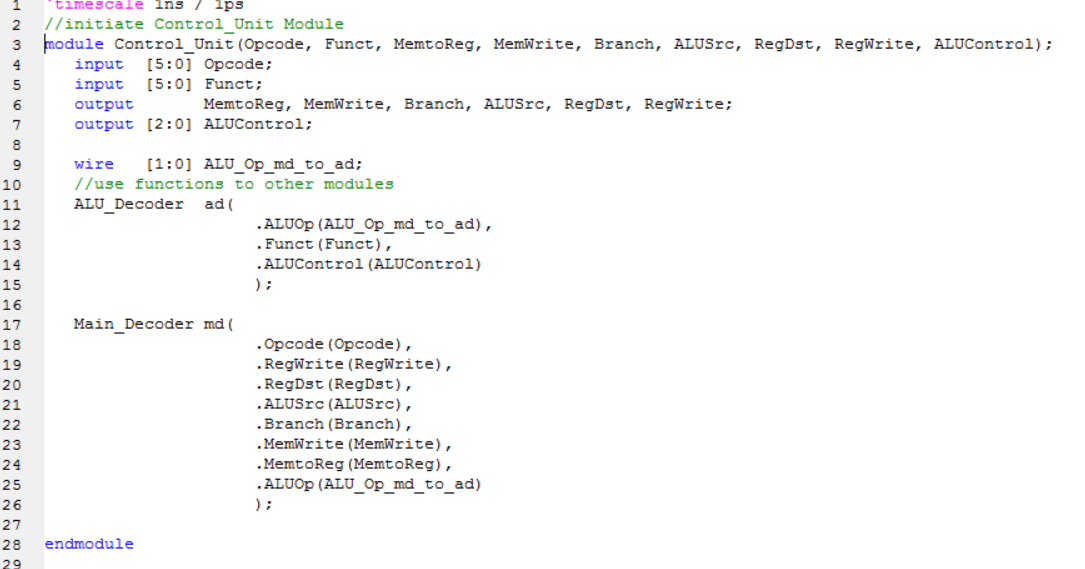
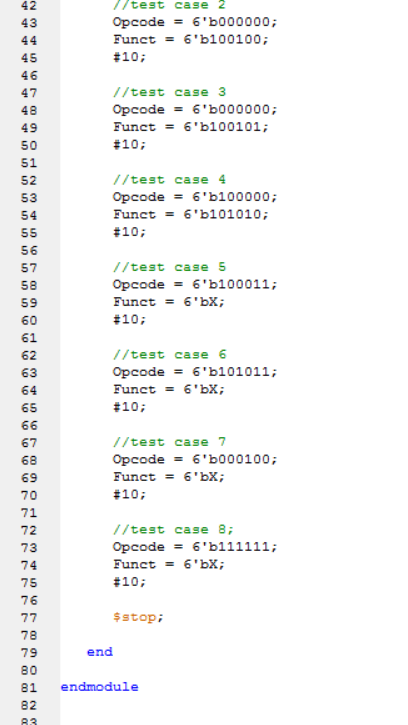
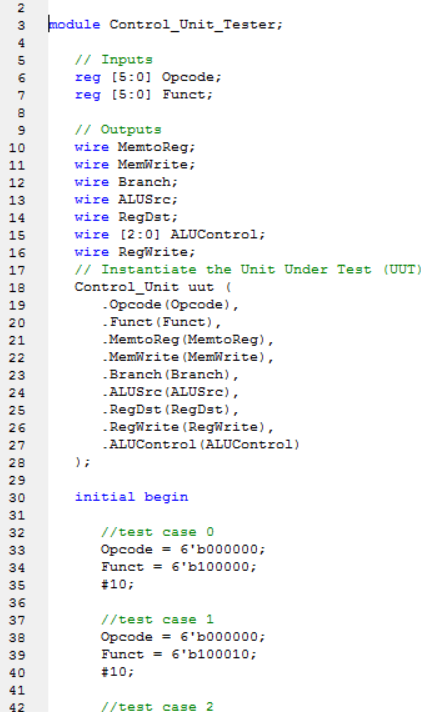
Lab 3

Eugene Paul Mesina



* **Section 1:** ALU\_Decoder Verilog module source



* **Section 2:** ALU\_Decoder Verilog Test Fixture
* **Section 3:** ALU\_Decoder Simulation Waveform Screenshot showing correct results
* **Section 4:** Main\_Decoder Verilog module source
* **Section 5:** Main\_Decoder Verilog Test Fixture
* **Section 6:** Main\_Decoder Simulation Waveform Screenshot showing correct results
* **Section 7:** Control\_Unit Verilog module source
* **Section 8:** Control\_Unit Verilog Test Fixture
* **Section 9:** Control\_Unit Simulation Waveform Screenshot showing correct results